IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	Application Number	**New Application**
	Filing Date	**Concurrently**
	First Named Inventor	**Atsushi ITO et al.**
	Group Art Unit	
	Examiner Name	
	Attorney Docket Number	**1596-186**
Title: **PLANAR DISPLAY PANEL CONTROLLER (As Amended)**		

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Please amend the subject application as follows prior to Examination on the Merits:

IN THE TITLE OF THE INVENTION:

Delete the current title of the invention and insert therefor:

--PLANAR DISPLAY PANEL CONTROLLER--

IN THE SPECIFICATION:

Page 1, between the title and the heading "TECHNICAL FIELD" insert

--CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of pending U.S. patent application Serial No. 09/194,118, filed November 23, 1998, which is a § 371 of PCT/JP98/01444, filed March 30, 1998.--

IN THE DISCLOSURE OF THE INVENTION:

Delete the paragraphs listed below and insert therefor the replacement paragraph shown on the pages following these instructions:

Page 8, fourth full paragraph;

Page 10, second paragraph;

Paragraph bridging pages 13 and 14.

As required by 37 C.F.R. § 1.121(b)(1)(iii), a marked-up version of each replacement paragraph showing all the changes relative to the previous version of the paragraph is attached to this amendment.

IN THE BRIEF DESCRIPTION OF THE DRAWINGS:

Delete the entire section headed "BRIEF DESCRIPTION OF THE DRAWINGS" and insert therefor the replacement section shown on the pages following these instructions.

As required by 37 C.F.R. §1.121(b)(2)(iii), a marked-up version of each replacement section showing all changes relative to the previous version of the section is attached to this amendment.

IN THE DETAILED DESCRIPTION:

Delete the paragraphs listed below and insert therefor the replacement paragraphs shown on the pages following these instructions:

Paragraph bridging pages 23 and 24;
Page 24, first full paragraph;
Page 24, second full paragraph;
Page 27, fourth full paragraph;
Page 27, fifth full paragraph;
Page 27, sixth full paragraph;
Page 28, first full paragraph;
Page 28, second full paragraph;
Page 28, third full paragraph;
Page 29, first full paragraph;
Page 32, first full paragraph;
Page 37, second paragraph;
Page 40, third paragraph;
Page 41, first full paragraph;
Page 41, second full paragraph;
Page 42, second paragraph;
Page 47, first full paragraph;
Paragraph bridging pages 49 and 50;

Page 53, fourth full paragraph;

Paragraph bridging pages 55 and 56;

Page 57, second full paragraph;

Paragraph bridging pages 58 and 59;

Page 59, first full paragraph;

Paragraph bridging pages 59 and 60;

Page 62, fourth full paragraph;

Page 64, second full paragraph;

Page 67, first full paragraph;

Paragraph bridging pages 71 and 72; and

Page 75, first full paragraph.

As required by 37 C.F.R. §1.121(b)(1)(iii), a marked-up version of each replacement paragraph showing all the changes relative to the previous version of the paragraph is attached to this amendment.

IN THE CLAIMS:

Please cancel claims 1-15 and 19-28 without prejudice or disclaimer.

REMARKS

The above amendments are being made to conform with U.S. practice.

Respectfully submitted,

By _____

George R. Repper, Reg. No. 31,414
Attorney for Applicant
ROTHWELL, FIGG, ERNST & MANBECK p.c.
Suite 701-E, 555 13th Street, N.W.
Washington, D.C. 20004
Telephone: (202)783-6040

Enclosures: Clean copy of Amended Sections of Specification
Marked-up version of Amended Sections of Specification

Clean Copy of BRIEF DESCRIPTION OF THE DRAWINGS:

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic view showing an entire construction of a planar display panel according to Embodiment 1 of the present invention,

Figs. 2A and 2B are partial perspective views showing a construction on a front glass substrate, as a first transparent substrate, which constitutes the display panel according to Embodiment 1 of the present invention,

Fig. 3 is a partial perspective view showing a construction on a back glass substrate, as a second substrate, which constitutes the display panel according to Embodiment 1 of the present invention,

Fig. 4 is a sectional view taken along line a - a' in Fig. 3,

Fig. 5 is a structural view showing evacuation grooves on the back glass substrate,

Fig. 6 is an explanatory view for explaining shapes of a lead pin 6 and a through hole 13 for leading out an electrode,

Fig. 7 is an explanatory view of a sealing guard 15 provided near a portion where the lead pins 6 are fused to the front glass substrate 1,

Figs. 8A, 8B and 8C are a set of views showing successive manufacturing steps of the front glass substrate 1,

Figs. 9A and 9B are a set of views showing successive manufacturing steps subsequent to Figs. 8A, 8B and 8C, Fig. 9C is an enlarged view of the circled portion in Fig. 9B,

Figs. 10A, 10B and 10C are a set of views showing successive manufacturing steps of the back glass substrate 10,

Figs. 11A, 11B and 11C are a set of views showing final steps of fitting the front glass substrate 1 and the back glass substrate 10 for assembly and sealing of the display panel,

Fig. 12 is an equivalent circuit diagram of the display panel, in which display cells are each represented by a discharge tube, for explaining a controller for the planar display panel according to Embodiment 2 of the present invention,

Fig. 13 is a block diagram of a driving circuit for explaining the controller for the planar display panel according to Embodiment 2 of the present invention,

Fig. 14 is a chart of driving waveforms applied to electrodes for display in luminance gradation by the driving circuit of Fig. 13,

Fig. 15 is a block diagram of a driving circuit showing a modification of Fig. 13,

Fig. 16A is a chart of driving waveforms applied to electrodes for display in luminance gradation by the driving circuit of Fig. 14, Fig. 16B is an enlarged view of the circled part of Fig. 16A, and Fig. 16C is an explanatory view for the waveforms,

Fig. 17 is a system block diagram of the planar display panel according to Embodiment 2 of the present invention,

Fig. 18 is a block diagram of a signal processing circuit for applying control signals to driving circuits of display modules cascaded in Fig. 17, for explaining the controller for the planar display panel according to Embodiment 2 of the present invention,

Fig. 19 is a waveform chart for explaining the operation of the signal processing circuit shown in Fig. 18,

Figs. 20A and 20B are a block diagram and a flowchart for explaining a gradation display process to create gradation data for control of individual electrodes using a pulse counter 56, a look-up table 57 and a display data generator 58 all shown in Fig. 18,

Fig. 21 is a graph of an input/output characteristic of the look-up table 57 shown in Fig. 18,

Fig. 22 is a block diagram of an individual electrode driving circuit for explaining a method for driving a planar display panel according to Embodiment 3 of the present invention,

Fig. 23 is a chart of a driving sequence for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Figs. 24A, 24B and 24C are explanatory views of the operation of the display panel for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Fig. 25 is an explanatory view of the operation of the display panel for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Figs. 26A, 26B and 26C are explanatory views of the initializing operation of the display cells for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Figs. 27A and 27B are explanatory views of the discharge operation for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Fig. 28 is a characteristic graph for control of the display cells for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Fig. 29 is a characteristic graph for control of the display cells for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Fig. 30 is a circuit diagram of a pulse generating circuit for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Fig. 31 is a characteristic graph for control of the display cells for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention, and

Fig. 32 is a timing chart for control of gradation display for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention.

Clean Copy of Replacement Paragraphs:

Page 8, Fourth Full Paragraph:

A fluorescent material layer is coated on a surface of the recess formed in the second substrate. Therefore, color display can be easily achieved with uniform luminance and hence uniformity of an image.

Page 10, Second Paragraph:

The lead pins are fused to the bus electrodes of the individual electrodes and the common electrode by a paste or bonding material which is comprised primarily of the same metallic material as that of the bus electrodes of the individual electrodes and the common electrode. Therefore, the lead pins can be firmly fixed to the electrodes.

Paragraph Bridging Pages 13 and 14:

In addition, the planar display panel is constituted by display modules as constituent elements each comprising a plurality of display units combined into a pattern of row-and-column matrix, the display modules arranged in the horizontal direction are cascaded, and a power supply is connected to the display modules in parallel. A signal processing circuit for applying control signals to the driving circuits of each of the display modules comprises an address information storage unit for storing specific address information, an input signal control unit for allowing input data to pass through it and taking data, which the display module including that control unit is to represent by itself, out of a position indicated by the specific address and a display effective signal in the data, a through data output buffer for outputting the data, which has passed through the input signal control unit, to the adjacent display module cascaded downstream, a memory into which the data taken out of the input signal control unit is written in response to a write control signal, and from which the data is read in response to a read control signal, a display pulse generator for generating common electrode and individual electrode driving pulses based on the data taken out of the input signal control unit, a counter for counting the common electrode driving pulse output from the display pulse generator, a look-up table for converting the number of pulses counted by the counter into a numerical value of gradation data, a display data generator for outputting individual electrode control data based on

comparison between the gradation data from the look-up table and the individual electrode driving display data read from the memory, and an output buffer for outputting signals of the display pulse generator and the display data generator to the individual electrode driving circuits and the common electrode driving circuits. Therefore, when data control is performed for the plurality of display modules combined with each other, individual control of the respective display modules in accordance with the display data can be achieved by taking in the display data corresponding to the address of each display module.

Paragraph Bridging Pages 23 and 24:

As shown in Fig. 2A, on one side of the front glass substrate 1, a pair of electrodes are provided in plural number in juxtaposed relation to form a group of electrodes, each pair comprising a common electrode 2 for driving all of display cells together, which constitute a display screen, or for partly driving any plural number of the display cells at a time, and one of individual electrodes 3 for individually driving the display cells on the cell-by-cell basis which constitute the display screen.

Page 24, First Full Paragraph:

A dielectric layer 4 and a protective film layer 5 are formed to cover the pairs of electrodes. An electrode leading-out lead pin 6 is vertically provided on each of the individual electrodes 3 in a position corresponding to between the display cells which constitute the display screen. Reference numeral 3b denotes a transparent electrode connected to a bus electrode 3a of the corresponding either individual electrode 3 or the common electrode 2.

Page 24, Second Full Paragraph:

Also, as shown in Fig. 2B, on one side of the front glass substrate 1, an electrode leading-out lead pin 7 is vertically provided on the common electrode 2 in a position corresponding to between the display cells similarly to the lead pin 6 for the individual electrode 3. The lead pins 6, 7 are fused to the common electrode 2 and the bus electrode 3a of the individual electrode 3 by a paste or blazing material which is comprised. primarily of the same metallic material as that of the common electrode 2 and the individual electrode 3. Note that, in

Fig. 2B which shows the vicinity of a portion where the lead pin for the common electrode 2 it taken out, broken lines represent electrode patterns underlying the dielectric layer 4.

Page 27, Fourth Full Paragraph:

First, as shown in Fig. 8A, the front glass substrate 1 having a transparent electrode for the individual electrodes formed all over one surface thereof is subjected to an etching step for patterning of the transparent electrode. A transparent electrode pattern is thus formed as shown in Fig. 8B.

Page 27, Fifth Full Paragraph:

Then, as shown in Fig. 8C, the bus electrodes of the individual electrodes 3 and the common electrode 2 are formed by screen printing.

Page 27, Sixth Full Paragraph:

Subsequently, as shown in Fig. 9A, the dielectric layer 4 made of an insulator and having windows for leading out the common electrode 2 and the individual electrodes 3 is formed by screen printing to cover the common electrode 2 and the individual electrodes 3.

Page 28, First Full Paragraph:

After that, as shown in Figs. 9B and 9C, the lead pins 6 and 7 are vertically fixed onto the common electrode 2 and the individual electrodes 3 through the electrode leading-out windows, followed by forming the protective film 5 by vacuum deposition.

Page 28, Third Full Paragraph:

First, the back glass substrate 10 shown in Fig. 10A is subjected to sand blasting to form recesses 11 defining the discharge spaces for the display cells which constitute the display screen on the back glass substrate, the electrode leading-out through holes 13a, 13b for leading out the lead pins 7, 6, respectively which are vertically fixed onto the common electrode 2 and the individual electrodes 3, to the back side of display screen, and the evacuation through holes 15 communicated with the evacuation grooves 14, as shown in Fig. 10B.

Page 28, Fourth Full Paragraph:

Then, as shown in Fig. 10C, the fluorescent material layers 12a, 12b, 12c in red, green and blue are coated by screen printing on the bottom surfaces of the recesses 11 forming the display cells with reflecting surfaces (not shown) of white glass or metal interposed therebetween.

Page 29, First Paragraph:

Next, as shown in Fig. 11A, the display panel is assembled by fitting the front glass substrate I and the back glass substrate 10, constructed as described above, to each other such that the lead pins 6 and 7 on the front glass substrate 1 are extended to the outside via the through holes 13 of the back glass substrate 10. Frit glass is applied to the assembled substrates to form sealing layers 16, as shown in Figs. 11B and 11C, thereby completing the sealed display panel. Incidentally, 17 denotes an evacuation glass tube.

Page 32, First Full Paragraph:

Since the lead pins are fused to the bus electrodes of the individual electrodes and the common electrode by a paste or bonding material which is comprised primarily of the same metallic material as that of the bus electrodes of the individual electrodes and the common electrode, the lead pins can be firmly fixed to the electrodes.

Page 37, Second Full Paragraph:

Basically, the display panel of this Embodiment can take only two states based on binary operation (whether to display or not) corresponding to an input pulse. Display is effected by applying a continuous display sustaining pulse, and a change of luminance (gradation) is controlled depending on the number of pulses which are applied to each of the individual electrodes within a unit time and insert in intervals between pulses applied to the common electrode.

Page 40, Third Paragraph:

More specifically, as shown in Fig. 16A, when maximum luminance is desired, all pulses are applied as the wide pulses to the individual electrode (see the waveform applied to the

individual electrode G11). On the other hand, for the cell requiring intermediate luminance, the narrow extinguishing pulses are applied from an intermediate point of the sequence (see the individual electrodes R11, G21).

Page 41, First Full Paragraph:

As shown in Fig. 16B in enlarged scale, the relatively wide sustaining pulse has a width of the sum of periods I and II, while the relatively narrow sustaining pulse has a width of the period I. Further, these periods I and II, a period III between the relatively wide sustaining pulse and the relatively narrow sustaining pulse, and a period IV after the relatively narrow sustaining pulse- are set by switching control of the total driving switch unit 21ab and the individual electrode driving switch unit 21aa, as shown in Fig. 16C.

Page 41, Second Full Paragraph:

For example, during the period I, the high-side PET and the low-side FET of the total driving switch unit 21ab are controlled to turn on and off, respectively, and the high-side FET and the low-side FET of the individual electrode driving switch unit 21aa are both controlled to turn off. Also, during the period II, the high-side FET and the low-side FET of the total driving switch unit 21ab are both controlled to turn off, and the high-side PET and the low-side FET of the individual electrode driving switch unit 21aa are controlled to turn on and off, respectively. Likewise, during the periods III and IV, the high-side FETs and the low-side FETs of the switch units 21ab, 21aa are controlled as shown in Fig. 16C.

Page 42, Second Full Paragraph: Version to show changes made

As shown in Fig. 17, a display section is constituted by a plurality of display modules 30 each being a constituent element and comprising four display units (2 x 2) of 8 x 8 dots combined with each other. The display modules 30 arranged in the horizontal direction (direction of scan line) are cascaded to be supplied with the same image and control signals in common.

Page 47, First Full Paragraph:

Figs. 20A and 20B are a block diagram and a flowchart for explaining a gradation display process to create gradation data for control of the individual electrodes using the pulse counter 56, the look-up table 57 and the display data generator 58 mentioned above.

Paragraph Bridging Pages 49 and 50:

More specifically, as shown in Fig. 20A, the display data generator 58 is constituted by comparators 58R, 58G, 58B of 8 bits. It is assumed, for example, that when the sustaining pulse is applied to effect discharge display, control data for the individual electrode is set to "1" (output of a display pulse), and when the control is to be performed to establish a non-display state, the control data is set to "0" (non-display state). Then, as shown in Fig. 20B, the pulse counter 56 comprising a 10-bit counter starts to count up the common electrode driving pulse output from the display pulse generator 55 upon counter reset (in synch with an vertical synch input), and the display data generator 58 compares a value *f* (the count number of sustaining pulses), which is resulted from converting an output of the pulse counter 56 by the look-up table 57, with the display image data, thereby obtaining the control data as follows;

if f ≤ display image data, then data is set to "1", and

if f > display image data, then data is set to "0".

The above comparing operation is repeated in number corresponding to the number of cells of the display module for each of the pulses applied to the individual electrodes until processing all the display data. The resulting data is successively transferred to the control pulse supply unit for switching control of the individual electrodes, shown in Fig. 13 or Fig. 15, so that whether to apply a pulse or not, a pulse shape, a voltage value, etc. for the next individual electrode are determined.

Page 53, Fourth Full Paragraph:

In planar display panels utilizing discharge, as shown in Figs. 24A, 24B and 24C, it is conventional that a high-voltage pulse is alternately applied to a pair of electrodes, i.e., a common electrode and one individual electrode opposing to the common electrode in the same plane in this embodiment, and discharge is sustained with the aide of wall charges accumulated on an insulator defining the discharge cell.

Paragraph Bridging Pages 55 and Page 56:

With the initializing pulses applied to the common electrode and the individual electrode, as shown in Figs. 26A, 26B and 26C, discharge is produced by the pulse applied to the common electrode in normal display as a result of the above-mentioned combination of the voltage pulses applied to the common electrode and the individual electrode. In the case where the pulse applied to the common electrode cannot bring about a dischargeable state, discharge is not produced by the voltage pulse applied to the common electrode, but produced by the voltage pulse applied to the individual electrode.

Page 57, Second Full Paragraph:

With such a phenomenon, as shown in Figs. 27A and 27B, there present no wall charges in the display cell after the pulse has been applied to the common electrode. Alternatively, even if present, the remaining wall charges are very weak. Accordingly, the wall charges have no longer an effect of impeding the occurrence of discharge when the next voltage pulse is applied to the common electrode. As a result, discharge is surely produced for each voltage pulse applied to the common electrode.

Paragraph Bridging Pages 58 and 59:

In this Embodiment 3, as shown in Figs. 27A and 27B, it was required that a period t1 from the rising of the first-step pulse to the rising of the second-step pulse was set to be not less than 1 μsec from relation between the on-time of a first-step pulse generating circuit and a second-step pulse generating circuit.

Page 59, First Full Paragraph:

Also, as shown in Figs. 27A and 27B, since the discharge starting voltage of the display cell is about 220 V, the first-step pulse having a voltage value V2 and the second-step pulse having a voltage value V1 each have a crest value of 160 V, whereby a voltage value resulted after superposing both the pulses is 320 V (V1 + V2).

Paragraph Bridging Pages 59 and 60:

The maximum voltage pulse applied at this time is set to have a voltage (320 V) allowing wall charges to be accumulated after the start of discharge in an amount enough to produce the erase discharge in the display cell, and a maximum voltage sustaining period t2 shown in Fig. 27A is set to be not less than 3 μsec that corresponds to a delay time in accumulation of the wall charges. Accordingly, the amount of wall charges enough to produce the erase discharge can be accumulated within the maximum voltage sustaining period t2.

Page 62, Fourth Full Paragraph:

The operation of the above circuit is now explained in more detail with reference to Fig. 30.

Page 64, Second Full Paragraph:

Further, transition states (②, ④, ⑥ and ⑧) between the successive conditions are continued for a period of about 0.5 μsec so that a penetrating current will not flow through the switching devices in push-pull connection. Pulse periods are determined by the periods of ①, ③, ⑤ and ⑦. The widths of those transition periods correspond to turning-on and turning-off times that are determined by respective switching devices (transistors or FETs) used.

Page 67, First Full Paragraph:

Here, luminance modulation (gradation display is performed in accordance with display data input from the outside. Supposing that display is to be made with luminance gradation in 256 steps like this Embodiment 3, pulses applied to the common electrode in times about 770 are allocated to 256 overlapping periods obtained by dividing one sequence, a certain number of divided periods is selected in accordance with the input data, and the discharge suppression voltage is applied to the individual electrode corresponding to the input data during the selected periods. As a result of the above operation, the display cell can make display with the luminance corresponding to the input display data.

Paragraph Bridging Pages 71 and Page 72:

As seen from the block diagram of gradation display control shown in Fig. 20A and a timing chart of the respective pulses shown in Fig. 32, input image data is stored in the image memory

in the number of pixels necessary for display, and the stored data is read in accordance with the display sequence. The data in the image memory is transferred to individual output control portions of the driving circuit for driving the individual electrodes in accordance with the position information of the display cells.

Page 75, First Full Paragraph:

In the above-described Embodiment 3, discharge is controlled by the switching operation using the crest value of the voltage 0 V or (discharge suppression voltage) applied to the individual electrode. However, the voltage applied tot he individual electrode or display control is not necessarily set to 0 V in the display period. By setting ;that voltage to a level as high as possible within the discharge region, a voltage difference required for the switching operation in display control is reduced and a driving circuit for lower voltage can be used. Where the first-step pulse and the second-step pulse constituting the composite voltage pulse applied to the common electrode are each set to have a voltage crest value of 160 V, for example, display control can be executed by applying the voltage applied to the individual electrode at a level of 50 V in the display period and 100 V in the non-display period.

Replacement section for BRIEF DESCRIPTION OF THE DRAWINGS: Version to show changes made

Fig. 1 is a schematic view showing an entire construction of a planar display panel according to Embodiment 1 of the present invention,

[Fig. 2 is a] Figs. 2A and 2B are partial perspective [view] views showing a construction on a front glass substrate, as a first transparent substrate, which constitutes the display panel according to Embodiment 1 of the present invention,

Fig. 3 is a partial perspective view showing a construction on a back glass substrate, as a second substrate, which constitutes the display panel according to Embodiment 1 of the present invention,

Fig. 4 is a sectional view taken along line a - a' in Fig. 3,

Fig. 5 is a structural view showing evacuation grooves on the back glass substrate,

Fig. 6 is an explanatory view for explaining shapes of a lead pin 6 and a through hole 13 for leading out an electrode,

Fig. 7 is an explanatory view of a sealing guard 15 provided near a portion where the lead pins 6 are fused to the front glass substrate 1,

[Fig. 8 is] Figs. 8A, 8B and 8C are a set of views showing successive manufacturing steps of the front glass substrate 1,

[Fig. 9 is] Figs. 9A and 9B are a set of views showing successive manufacturing steps subsequent to [Fig. 8,] Figs. 8A, 8B and 8C, Fig. 9C is an enlarged view of the circled portion in Fig. 9B,

[Fig. 10 is] Figs. 10A, 10B and 10C are a set of views showing successive manufacturing steps of the back glass substrate 10,

[Fig. 11 is] Figs. 11A, 11B and 11C are a set of views showing final steps of fitting the front glass substrate 1 and the back glass substrate 10 for assembly and sealing of the display panel,

Fig. 12 is an equivalent circuit diagram of the display panel, in which display cells are each represented by a discharge tube, for explaining a controller for the planar display panel according to Embodiment 2 of the present invention,

Fig. 13 is a block diagram of a driving circuit for explaining the controller for the planar display panel according to Embodiment 2 of the present invention,

Fig. 14 is a chart of driving waveforms applied to electrodes for display in luminance gradation by the driving circuit of Fig. 13,

Fig. 15 is a block diagram of a driving circuit showing a modification of Fig. 13,

Fig. 16A is a chart of driving waveforms applied to electrodes for display in luminance gradation by the driving circuit of Fig. 14, [including] Fig. 16B is an enlarged view of the circled part of Fig. 16A, and Fig. 16C is an explanatory view for the waveforms,

Fig. 17 is a system block diagram of the planar display panel according to Embodiment 2 of the present invention,

Fig. 18 is a block diagram of a signal processing circuit for applying control signals to driving circuits of display modules cascaded in Fig. 17, for explaining the controller for the planar display panel according to Embodiment 2 of the present invention,

Fig. 19 is a waveform chart for explaining the operation of the signal processing circuit shown in Fig. 18,

[Fig. 20 is a combination of] Figs. 20A and 20B are a block diagram and a flowchart for explaining a gradation display process to create gradation data for control of individual electrodes using a pulse counter 56, a look-up table 57 and a display data generator 58 all shown in Fig. 18,

Fig. 21 is a graph of an input/output characteristic of the look-up table 57 shown in Fig. 18,

Fig. 22 is a block diagram of an individual electrode driving circuit for explaining a method for driving a planar display panel according to Embodiment 3 of the present invention,

Fig. 23 is a chart of a driving sequence for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

[Fig. 24 is an] Figs. 24A, 24B and 24C are explanatory [view] views of the operation of the display panel for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Fig. 25 is an explanatory view of the operation of the display panel for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

[Fig. 26 is an] Figs. 26A, 26B and 26C are explanatory [view] views of the initializing operation of the display cells for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

[Fig. 27 is an] Figs. 27A and 27B are explanatory [view] views of the discharge operation for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Fig. 28 is a characteristic graph for control of the display cells for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Fig. 29 is a characteristic graph for control of the display cells for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Fig. 30 is a circuit diagram of a pulse generating circuit for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention,

Fig. 31 is a characteristic graph for control of the display cells for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention, and

Fig. 32 is a timing chart for control of gradation display for explaining the method for driving the planar display panel according to Embodiment 3 of the present invention.

Replacement Paragraphs: Version to show changes made

Page 8, Fourth Full Paragraph: Version to show changes made

A fluorescent material layer is coated on a [bottom] surface of the recess formed in the second substrate. Therefore, color display can be easily achieved with uniform luminance and hence uniformity of an image.

Page 10, Second Paragraph: Version to show changes made

The lead pins are fused to the bus electrodes of the individual electrodes and the common electrode by a paste or [blazing] bonding material which is comprised primarily of the same metallic material as that of the bus electrodes of the individual electrodes and the common electrode. Therefore, the lead pins can be firmly fixed to the electrodes.

Paragraph Bridging Pages 13 and 14: Version to show changes made

In addition, the planar display panel is constituted by display modules as constituent elements each comprising a plurality of display units combined into a pattern of row-and-column matrix, the display modules arranged in the horizontal direction are cascaded, and a power supply is connected to the display modules in parallel. A signal processing circuit for applying control signals to the driving circuits of each of the display modules comprises an address information storage unit for storing specific address information, an input signal control unit for allowing input data to pass through it and taking data, which the display module including that control unit is to represent by itself, out of a position indicated by the specific address and a display effective signal in the data, a through data output buffer for outputting the data, which has passed through the input signal control unit, to the adjacent display module cascaded downstream, a memory into which the data taken out of the input signal control unit is written in response to a write control signal, and from which the data is read in response to a read control signal, a display pulse generator for generating common electrode and individual electrode driving pulses based on the data taken out of the input signal control unit, a counter for counting the common electrode driving pulse output from the display pulse generator, a look-up table for converting the number of pulses counted by the counter into a numerical value of gradation data, a display data generator for outputting individual electrode control data based on

comparison between the gradation data from the look-up table and the individual electrode driving display data read from the memory, and an output buffer for outputting [outputs] signals of the display pulse generator and the display data generator to the individual electrode driving circuits and the common electrode driving circuits. Therefore, when data control is performed for the plurality of display modules combined with each other, individual control of the respective display modules in accordance with the display data can be achieved by taking in the display data corresponding to the address of each display module.

Paragraph Bridging pages 23 and 24: Version to show changes made

As shown in [Fig. 2(a)] Fig. 2A, on one side of the front glass substrate 1, a pair of electrodes are provided in plural number in juxtaposed relation to form a group of electrodes, each pair comprising a common electrode 2 for driving all of display cells together, which constitute a display screen, or for partly driving any plural number of the display cells at a time, and one of individual electrodes 3 for individually driving the display cells on the cell-by-cell basis which constitute the display screen.

Page 24, First Full Paragraph: Version to show changes made

A dielectric layer 4 and a protective film layer 5 are formed to cover the pairs of electrodes. An electrode leading-out lead pin is vertically provided on each of the individual electrodes 3 in a position corresponding to between the display cells which constitute the display screen. Reference numeral 3b denotes a transparent electrode connected to a bus electrode 3a of the corresponding either individual electrode 3 [and] or the common electrode 2.

Page 24, Second Full Paragraph: Version to show changes made

Also, as shown in [Fig. 2(b)] Fig. 2B, on one side of the front glass substrate 1, an electrode leading-out lead pin 7 is vertically provided on the common electrode 2 in a position corresponding to between the display cells similarly to the lead pin 6 for the individual electrode 3. The lead pins 6, 7 are fused to the [common electrode 2 and the] bus electrode 3a of the individual electrode 3 and the common electrode 2 by a paste or blazing material which is comprised. primarily of the same metallic material as that of the common electrode 2 and the individual electrode 3. Note that, in [Fig. 2(b)] Fig. 2B which shows the vicinity of a portion

where the lead pin for the common electrode 2 it taken out, broken lines represent electrode patterns underlying the dielectric layer 4.

Page 27, Fourth Full Paragraph: Version to show changes made

First, as shown in [Fig. 8(a)] Fig. 8A, the front glass substrate 1 having a transparent electrode for the individual electrodes formed all over one surface thereof is subjected to an etching step for patterning of the transparent electrode. A transparent electrode pattern is thus formed as shown in [Fig. 8(b)] Fig. 8B.

Page 27, Fifth Full Paragraph: Version to show changes made

Then, as shown in [Fig. 8(c)] Fig. 8C, the bus electrodes of the individual electrodes 3 and the common electrode 2 are formed by screen printing.

Page 27, Sixth Full Paragraph: Version to show changes made

Subsequently, as shown in [Fig. 9(d)] Fig. 9A, the dielectric layer 4 made of an insulator and having windows for leading out the common electrode 2 and the individual electrodes 3 is formed by screen printing to cover the common electrode 2 and the individual electrodes 3.

Page 28, First Full Paragraph: Version to show changes made

After that, as shown in [Fig. 9(e)] Figs. 9B and 9C, the lead pins 6 and 7 are vertically fixed onto the common electrode 2 and the individual electrodes 3 through the electrode leading-out windows, followed by forming the protective film layer 5 layer by vacuum deposition.

Page 28, Third Full Paragraph: Version to show changes made

First, the back glass substrate 10 shown in [Fig. 10(a)] Fig. 10A is subjected to sand blasting to form recesses 11 defining the discharge spaces for the display cells which constitute the display screen on the back glass substrate, the electrode leading-out through holes 13a, 13b for leading out the lead pins 7, 6, respectively which are vertically fixed onto the common electrode 2 and the individual electrodes 3, to the back side of display screen, and the evacuation through holes 15 communicated with the evacuation grooves 14, as shown in [Fig. 10(b)] Fig. 10B.

Page 28, Fourth Full Paragraph: Version to show changes made

Then, as shown in [Fig. 10(c)] Fig. 10C, the fluorescent material layers 12a, 12b, 12c in red, green and blue are coated by screen printing on the bottom surfaces of the recesses 11 forming the display cells with reflecting surfaces (not shown) of white glass or metal interposed therebetween.

Page 29, First Paragraph: Version to show changes made

Next, as shown in [Fig. 11(a)] Fig. 11A, the display panel is assembled by fitting the front glass substrate I and the back glass substrate 10, constructed as described above, to each other such that the lead pins 6 and 7 on the front glass substrate 1 are extended to the outside via the through holes 13 of the back glass substrate 10. Frit glass is applied to the assembled substrates to form sealing layers 16, as shown in [Fig. 11(b)] Figs. 11B and 11C, thereby completing the sealed display panel. Incidentally, 17 denotes an evacuation glass tube.

Page 32, First Full Paragraph: Version to show changes made

Since the lead pins are fused to the bus electrodes of the individual electrodes and the common electrode by a paste or [blazing] bonding material which is comprised primarily of the same metallic material as that of the bus electrodes of the individual electrodes and the common electrode, the lead pins can be firmly fixed to the electrodes.

Page 37, Second Full Paragraph: Version to show changes made

Basically, the display panel of this Embodiment can take only two states based on binary operation (whether to display or not) corresponding to an input pulse. [Therefore, the display panel cannot change luminance depending on the amplitude of the pulse itself.] Display is effected by applying a continuous display sustaining pulse, and a change of luminance (gradation) is controlled depending on the number of pulses which are applied to each of the individual electrodes within a unit time and insert in intervals between pulses applied to the common electrode.

Page 40, Third Paragraph: Version to show changes made

More specifically, as shown in [Fig. 16(a)] Fig. 16A, when maximum luminance is desired, all pulses are applied as the wide pulses to the individual electrode (see the waveform applied to the individual electrode G11). On the other hand, for the cell requiring intermediate luminance, the narrow extinguishing pulses are applied from an intermediate point of the sequence (see the individual electrodes R11, G21).

Page 41, First Full Paragraph: Version to show changes made

As shown in [part of Fig. 16 (a)] Fig. 16B in enlarged scale, the relatively wide sustaining pulse has a width of the sum of periods I and II, while the relatively narrow sustaining pulse has a width of the period I. Further, these periods I and II, a period III between the relatively wide sustaining pulse and the relatively narrow sustaining pulse, and a period IV after the relatively narrow sustaining pulse- are set by switching control of the total driving switch unit 21ab and the individual electrode driving switch unit 21aa, as shown in [Fig. 16(b)] Fig. 16C.

Page 41, Second Full Paragraph: Version to show changes made

For example, during the period I, the high-side PET and the low-side FET of the total driving switch unit 21ab are controlled to turn on and off, respectively, and the high-side FET and the low-side FET of the individual electrode driving switch unit 21aa are both controlled to turn off. Also, during the period II, the high-side FET and the low-side FET of the total driving switch unit 21ab are both controlled to turn off, and the high-side PET and the low-side FET of the individual electrode driving switch unit 21aa are controlled to turn on and off, respectively. Likewise, during the periods III and IV, the high-side FETs and the low-side FETs of the switch units 21ab, 21aa are controlled as shown in [Fig. 16(b)] Fig. 16C.

Page 42, Second Full Paragraph: Version to show changes made

As shown in Fig. 17, a display section is constituted by a plurality of display modules 30 each being a constituent element and comprising four display units (2 x 2) of 8 x 8 dots combined with each other. The display modules 30 arranged in the horizontal direction (direction of scan line) are cascaded to be supplied with the same image and control signals in common.

Page 47, First Full Paragraph: Version to show changes made

[Figs. 20(a) and 20(b)] Figs. 20A and 20B are a block diagram and a flowchart for explaining a gradation display process to create gradation data for control of the individual electrodes using the pulse counter 56, the look-up table 57 and the display data generator 58 mentioned above.

Paragraph Bridging Pages 49 and 50: Version to show changes made

More specifically, as shown in [Fig. 20(a)] Fig. 20A, the display data generator 58 is constituted by comparators 58R, 58G, 58B of 8 bits. It is assumed, for example, that when the sustaining pulse is applied to effect discharge display, control data for the individual electrode is set to "1" (output of a display pulse), and when the control is to be performed to establish a non-display state, the control data is set to "0" (non-display state). Then, as shown in [Fig. 20(b)] Fig. 20B, the pulse counter 56 comprising a 10-bit counter starts to count up the common electrode driving pulse output from the display pulse generator 55 upon counter reset (in synch with an vertical synch input), and the display data generator 58 compares a value *f* (the count number of sustaining pulses), which is resulted from converting an output of the pulse counter 56 by the look-up table 57, with the display image data, thereby obtaining the control data as follows;

if f ≤ display image data, then data is set to "1", and

if f > display image data, then data is set to "0".

The above comparing operation is repeated in number corresponding to the number of cells of the display module for each of the pulses applied to the individual electrodes until processing all the display data. The resulting data is successively transferred to the control pulse supply unit for switching control of the individual electrodes, shown in Fig. [21] 13 or Fig. 15, so that whether to apply a pulse or not, a pulse shape, a voltage value, etc. for the next individual electrode are determined.

Page 53, Fourth Full Paragraph: Version to show changes made

In planar display panels utilizing discharge, as shown in [Fig. 24] Figs. 24A, 24B and 24C, it is conventional that a high-voltage pulse is alternately applied to a pair of electrodes, i.e., a common electrode and one individual electrode opposing to the common electrode in the

same plane in this embodiment, and discharge is sustained with the aide of wall charges accumulated on an insulator defining the discharge cell.

Paragraph Bridging Pages 55 and Page 56: Version to show changes made

With the initializing pulses applied to the common electrode and the individual electrode, as shown in [Fig. 26,] Figs. 26A, 26B and 26C, discharge is produced by the pulse applied to the common electrode in normal display as a result of the above-mentioned combination of the voltage pulses applied to the common electrode and the individual electrode. In the case where the pulse applied to the common electrode cannot bring about a dischargeable state, discharge is not produced by the voltage pulse applied to the common electrode, but produced by the voltage pulse applied to the individual electrode.

Page 57, Second Full Paragraph: Version to show changes made

With such a phenomenon, as shown in [Fig. 27] Figs. 27A and 27B, there present no wall charges in the display cell after the pulse has been applied to the common electrode. Alternatively, even if present, the remaining wall charges are very weak. Accordingly, the wall charges have no longer an effect of impeding the occurrence of discharge when the next voltage pulse is applied to the common electrode. As a result, discharge is surely produced for each voltage pulse applied to the common electrode.

Paragraph Bridging Pages 58 and 59: Version to show changes made

In this Embodiment 3, as shown in [Fig. 27,] Figs. 27A and 27B, it was required that a period t1 from the rising of the first-step pulse to the rising of the second-step pulse was set to be not less than 1 μsec from relation between the on-time of a first-step pulse generating circuit and a second-step pulse generating circuit.

Page 59, First Full Paragraph: Version to show changes made

Also, as shown in [Fig. 27,] Figs. 27A and 27B, since the discharge starting voltage of the display cell is about 220 V, the first-step pulse having a voltage value V2 and the

second-step pulse having a voltage value V1 each have a crest value of 160 V, whereby a voltage value resulted after superposing both the pulses is 320 V (V1 + V2).

Paragraph Bridging Pages 59 and 60: Version to show changes made

The maximum voltage pulse applied at this time is set to have a voltage (320 V) allowing wall charges to be accumulated after the start of discharge in an amount enough to produce the erase discharge in the display cell, and a maximum voltage sustaining period t2 shown in [Fig. 27] Fig. 27A is set to be not less than 3 μsec that corresponds to a delay time in accumulation of the wall charges. Accordingly, the amount of wall charges enough to produce the erase discharge can be accumulated within the maximum voltage sustaining period t2.

Page 62, Fourth Full Paragraph: Version to show changes made

The operation of the above circuit is now explained in more detail with reference to Fig. [5] 30.

Page 64, Second Full Paragraph: Version to show changes made

Further, transition states ([⑨]②, ④, ⑥ and ⑧) between the successive conditions are continued for a period of about 0.5 μsec so that a penetrating current will not flow through the switching devices in push-pull connection. Pulse periods are determined by the periods of ①, ③, ⑤ and [⑨]⑦. The widths of those transition periods correspond to turning-on and turning-off times that are determined by respective switching devices (transistors or FETs) used.

Page 67, First Full Paragraph: Version to show changes made

Here, luminance modulation (gradation display is performed in accordance with display data input from the outside. Supposing that display is to be made with luminance gradation in 256 steps like this Embodiment 3, pulses applied to the common electrode in times [at maximum] about 770 are allocated to 256 overlapping periods obtained by dividing one sequence, a certain number of divided periods is selected in accordance with the input data, and the discharge suppression voltage is applied to the individual electrode corresponding to the input data during the selected periods. As a result of the above operation, the display cell can make display with the luminance corresponding to the input display data.

Paragraph Bridging Pages 71 and Page 72: Version to show changes made

As seen from the block diagram of gradation display control shown in [Fig. 20] Fig. 20A and a timing chart of the respective pulses shown in Fig. 32, input image data is stored in the image memory in the number of pixels necessary for display, and the stored data is read in accordance with the display sequence. The data in the image memory is transferred to individual output control portions of the driving circuit for driving the individual electrodes in accordance with the position information of the display cells.

Page 75, First Full Paragraph: Version to show changes made

In the above-described Embodiment 3, discharge is controlled by the switching operation using the crest value of the voltage [applied to the individual electrode in the range of 0 V -] 0 V or (discharge suppression voltage) applied to the individual electrode. However, the voltage applied tot he individual electrode or display control is not necessarily set to 0 V in the display period. By setting ;that voltage to a level as high as possible within the discharge region, a voltage difference required for the switching operation in display control is reduced and a driving circuit for lower voltage can be used. Where the first-step pulse and the second-step pulse constituting the composite voltage pulse applied to the common electrode are each set to have a voltage crest value of 160 V, for example, display control can be executed by applying the voltage applied to the individual electrode at a level of 50 V in the display period and 100 V in the non-display period.